REMARKS

Claims 1-19 were pending in the application prior to the present amendment.
Claims 4 and 13 are herein cancelled.
Claims 1, 5, 6, 11, 14 and 16-19 are herein amended.
Claim 20 has been added. Claim 20 is identical to former Claim 11.
Thus, Claims 1-3, 5-12 and 14-19 will be pending in the application after entry of the present amendment.

Allowable Claims

Claims 8-10 and 13-15 were indicated to be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Therefore, claim 11 has been amended to include the subject matter of former claim 13. Independent claims 18 and 19 have also been amended to include the features of claim 13, and thus, are believed to be allowable.

Art Rejections

Claims 1, 4-5 and 16-17 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Horton (U.S. Patent No. 6,421,696).

Claims 6, 11 and 18-19 were rejected under 35 U.S.C. Section 103(a) as being obvious over Horton (U.S. Patent No. 6,421,696) in view of Hung et al. ("Statistical Inverse Discrete Cosine Transforms for Image Compression").

Claims 2-3, 7 and 12 were rejected under 35 U.S.C. Section 103(a) as being obvious over Horton (U.S. Patent No. 6,421,696), as applied to claim 1 above, in view of Advanced Micro Devices Inc. ("AMD Extensions to the 3DNow!™ and MMX™ Instructions Sets Manual").

These rejections are respectfully traversed based on the following reasoning.

Claim 1 as amended herein recites:

> "A method of performing a two-dimensional discrete cosine transform (DCT) using a microprocessor having an instruction set that includes single-

instruction multiple-data (SIMD) floating point instructions, wherein the method comprises: receiving a block of integer data having C columns and R rows, wherein each of the R rows contains C row data values, wherein the block of integer data is indicative of a portion of an image; and
for each row,
loading the C row data values of the row into registers;
converting the C row data values into floating point form, wherein the registers each hold two floating point row data values; and
performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations are performed using SIMD floating point instructions;
altering the arrangement of values in the registers;
performing a second plurality of weighted-rotation operations on the values in the registers;
again altering the arrangement of the values in the registers;
performing a third plurality of weighted-rotation operations on the values in the registers;
yet again altering the arrangement of the values in the registers; and
performing a fourth plurality of weighted-rotation operations on the values in the registers to obtain intermediate floating point values."

This combination of features is not taught or suggested in Horton. In particular, Horton never teaches or suggests altering the arrangement of values in the registers three times between performances of weighted-rotation operations as recited in claim 1. The Examiner relies on Horton Figures 1 and 10 to teach alterations of arrangement between performances of weighted-rotation operations. Figure 1 is a signal flow graph illustrating multiple passes where each pass includes a collection of butterfly operations. Figure 10 is a signal flow graph illustrating the computation of a single group within an intermediate pass. Neither of these Figures teaches or suggests alterations of the arrangement of values in the registers between performances of weighted-rotation operations as recited in claim 1.

Furthermore, claim 1 recites that "each of the R rows contains C row data values" and "for each row, loading the C row data values into registers ...". Thus, the method of claim 1 comprises loading an entire row of data values into registers. Horton nowhere teaches or suggests this feature. The Examiner relies on Figure 6 and Col. 2, lines 44-50 to teach this feature. Figure 6 illustrates "a data array 700 which stores initial FFT operands and intermediate computations results as well as the final output of the FFT algorithm". (Col. 6, lines 32-34) Figure 6 in no way suggests that an entire row of data values from a received block are loaded into registers as recited in claim 1. Col. 2, lines 44-50 recite:

> "Furthermore, suppose that the input array comprises eight samples of a signal X. Thus, the eight samples may be represented as X(000), X(001), X(010), X(011), X(100), X(101), X(110) and X(111) in the order they appear in the input array. The FFT algorithm accesses these input values in the order X(000), X(100), X(010), X(110), X(001), X(101), X(011) and X(111). Coley and Tukey realized that the addresses of samples in the access order and the memory order were effectively bit reversed."

This passage in no way suggests that an entire row of data values from a received block are loaded into registers as recited in claim 1.

Thus, claim 1 and its dependents are patentably distinguished over Horton at least for the reasons give above.

Claims 16 and 17 as amended herein recite features similar to those recited in Claim 1. Thus, Claims 16 and 17 are patentably distinguished over Horton for reasons similar to those advanced above.

Claim 6 recites "<u>for two columns at a time</u>: loading data from two columns of intermediate data into each of a plurality of registers; and performing a plurality of weighted-rotation operations on the values in the registers, wherein the weighted-rotation operations for two columns are performed in parallel using SIMD floating point instructions." The Examiner relies on Hung et al. Figures 2 and 4 to disclose these features. Figure 2 illustrates eight input values being operated on to generate eight output values. The even and odd input values are operated on by separate AAN IDCT operators. Figure 4 illustrates a simplification for the odd IDCT operator. These Figures in no way suggest the recited features of Claim 6. Thus, claim 6 and its dependents are patentably distinguished over Horton and Hung et al. Claims 11, 18, 19 and 20 are similarly distinguished over Horton and Hung et al.

<u>CONCLUSION</u>

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant hereby petitions for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 501505/5500-59800/BNK. Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Request for Approval of Drawing Changes

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $___ for fees (   ).

Respectfully submitted,

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